A Low-Power Highly Linear Cascoded Multiple-Gated Transistor CMOS RF Amplifier With 10 dB IP3 Improvement (Revised*)

Tae Wook Kim, Bonkee Kim, Ilku Nam, Beomkyu Ko, and Kwyro Lee

***Abstract*—A low-power highly linear CMOS RF amplifier circuit composed of a Multiple-Gated common-source FET TRansistor (MGTR) in cascode configuration is reported. In a MGTR amplifier, linearity is improved by using transconductance linearization which can be achieved by canceling the negative peak value of g_m'' of the main transistor with the positive one in the auxiliary transistor having a different size and gate drive combined in parallel. This enhancement, however, is limited by the distortion originated from the combined influence of g_m' and harmonic feedback, which can greatly be reduced by the cascoding MGTR output. IP3 improvement as large as 10 dB has been obtained from an experimental RF amplifier designed at 900 MHz and fabricated using 0.35 μm BiCMOS technology using only CMOS at a similar power consumption and gain as those obtainable from conventional cascode single gate transistor amplifiers.**

***Index Terms*—CMOS, IP3, MGTR, nonlinearity.**

I. Introduction

MODERN communication systems, such as, WCDMA, GSM, Bluetooth, etc., require high performance, low-power and highly linear integrated RF circuits. For a RF amplifier, the linearity requirement becomes more and more stringent, not only for power amplifier/drive amplifiers but also for LNA and mixers in the receiver circuit. The linearity of the power/drive amplifier has a strong influence on the ACPR (adjacent channel power ratio), and that of the LNA and mixer directly related to the immunity to the various interferences.

It was shown in previous work [1], that we can achieve high linearity without using extra power by canceling the third order nonlinearity coefficient, g_m'', by using MGTR. With properly adjusted gate width and gate drive voltage $(V_{gs}-V_{th})$ of the Auxiliary Transistor (AT), the nonlinear characteristics of the Main Transistor (MT) can be compensated for. In [1], the authors obtained appreciable improvement in IIP3 (input referred third order distortion) or OIP3 (output referred third order distortion) at similar power consumption and gain as those obtainable from a conventional single gate transistor amplifier. However, this enhancement is much less than that expected from the improvement in g_m''. Soon after, one of the authors figured out that g_m'' cancelation alone cannot increase IIP3 or OIP3 by more than 3–4 dB, because the other nonlinear distortion originated from the finite value of g_m' combined with the harmonic feedback becomes dominant [2]. Using Volterra series analysis, he found that the sub-harmonic and second harmonic components play a dominant role in limiting linearity enhancement in the g_m''-canceled MGTR amplifier. Based on this analysis, he proposed that, with proper second harmonic termination, it is indeed possible to achieve order of magnitude of linearity enhancement.

In this paper, an experimental 900 MHz RF CMOS amplifier circuit with linearity improvement as large as 10 dB is reported, adapting above mentioned approaches, i.e., MGTR combined with cascode configuration. We show IIP3 analysis of a common-source FET (CSFET) amplifier in the next section, which is followed by the design, fabrication and linearity measurement result of an experimental CMOS amplifier using 0.35 μm BiCMOS technology.

Linearization methods in system level have been published such as, pre-distortion [3], feedforward error-cancelation [4] and Cartesian feedback [5]. But those methods are not suitable for handset application because of complex hardware. For handset application, use of an auxiliary triode region MOSFET to compensate for the nonlinearity of the main RF amplifier [6] and 3rd order harmonic canceling [7] were proposed. However, those methods increase dc power consumption with its additional circuits. Too much power consumption (150 mA) [6] because of using triode region and too low-power gain [7] are not suitable for application.

II. IIP3 Analysis of Cascoded MGTR CMOS Amplifier

CSFET amplifier nonlinearity mostly comes from transconductance (g_m) nonlinearity in the driving MOSFET transistor. For example, that of third order intermodulation distortion (IMD3) is mainly determined by the value of the second derivative of transconductance [1].

As was shown before in [1], that g_m'' has a negative peak value in the gate drive voltage range of 0.1$\sim$0.4 V where MOSFET amplifier is usually biased for low-power application. Thus, linearity degradation is quite severe. In the MGTR amplifier, however, this negative peak of MT can be canceled by the positive peak value of properly sized AT whose transfer characteristics

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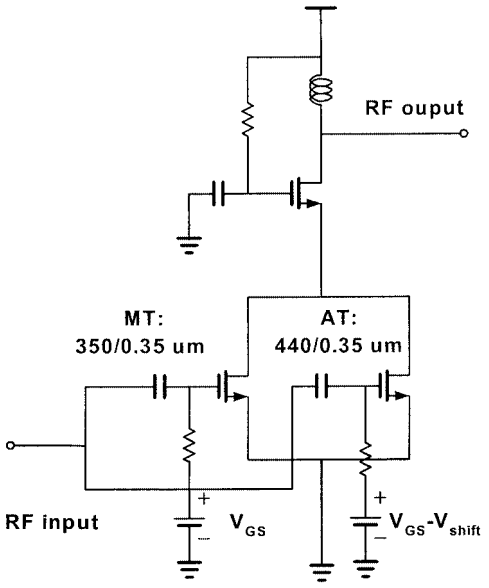

Fig. 1. MGTR with cascode configuration.

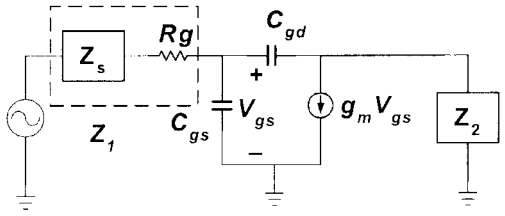

Fig. 2. Analyzed common source equivalent circuit.

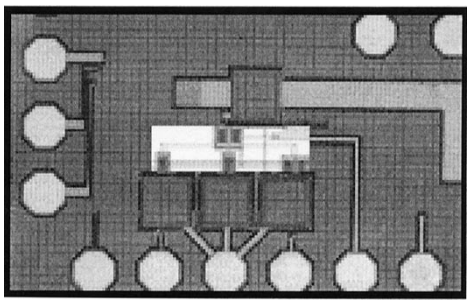

Fig. 3. Chip microphotograph.

can be shifted to the right by changing either the gate bias or the threshold voltage. Note that this linearization method does not require extra power consumption, because AT is biased in subthreshold regime. In MGTR linearization, the need for its multiple-gate voltages for multiple auxiliary transistors could increase bias circuitry complexity. However, one or two auxiliary transistors are enough for linearization and with its immunity to process variation as shown in Section III, conventional current source bias circuit is enough for auxiliary transistor bias circuit, thus bias circuit complexity may not be a burden.

The effect of out-of-band termination on intermodulation distortion was originally analyzed for a bipolar common emitter amplifier circuit [8], which can be applied FET one as follows:

$$IIP3 = \frac{1}{6\mathrm{Re}[Z_s(\omega)]\cdot|H(\omega)|\cdot|A_1(\omega)|^3|\varepsilon(\Delta\omega,\,2\omega)|} \quad (1)$$

$$\varepsilon(\Delta\omega,\,2\omega) = g_m'' - g_{OB} \quad (2)$$

where

$$g_{OB} = \frac{2(g_m')^2}{3}\left[\frac{2}{g_m + g(\Delta\omega)} + \frac{1}{g_m + g(2\omega)}\right]. \quad (3)$$

Here, Z_s indicates the source impedance and $g(\Delta\omega)$ and $g(2\omega)$ are the linearity related terms at $\Delta\omega$ and 2ω respectively. For the meaning of $H(\omega)$ and $A_1(\omega)$, refer to the original paper [2]. Equations (1)–(3) implies that linearity (IIP3 or OIP3) improvement can indeed be improved by reducing g_m'', but that, as can be seen in (2), when g_m'' becomes small, $\varepsilon(\Delta\omega, 2\omega)$ becomes dominated by g_{OB} which is proportional to the square of g_m' [see (3)]. However, although g_m'' peak can effectively be canceled using MGTR, the value of g_m' is still appreciable [2]. Therefore, we have to devise some way to decrease g_{OB}. One of the best ways to achieve this is to increase both $g(\Delta\omega)$ and $g(2\omega)$.

In CSFET circuit as shown in Fig. 1. $g(2\omega)$ was originally defined in [8], which can be approximately given as

$$g(2\omega) \approx g_m \times \frac{1 + 2j\omega C_{gs}Z_1 + 2j\omega C_{gd}Z_2}{1 + \omega_T C_{gd} Z_2}. \quad (4)$$

Here, Z_1 and Z_2 are the impedance looking into the source and that into the load (see Fig. 2) respectively and is the unit current cutoff angular frequency defined as $\omega_r = g_m/C_{gs}$. Note that $g(\Delta\omega)$ is much larger compared with $g(2\omega)$.

In a typical CSFET amplifier, the magnitude of Z_1 is of the order of $1/(\omega C_{gs})$. Thus, the second term in the numerator of (4) is comparable to 1. Furthermore, $2\omega \ll \omega_T$, implies that $\omega_T C_{gd} Z_2$ in the denominator is the most dominating factor. Therefore, it is very important to reduce $\omega_T C_{gd} Z_2$ smaller than 1. In other words, Z_2 should be decreased as much as possible. In ref.[8] harmonic tuning is used to decrease Z_2. In this paper, however, we propose to use cascode configuration to reduce Z_2. In cascode configuration Z_2 is decreased to $1/g_m$. Although this is not as good as the harmonic tuning, our approach is more plausible because it provides as good as performance as the harmonic tuning method and does not require large passive components as in [8]. In summary, in the MGTR amplifier, IP3 increases firstly by decreased g_m'' in $\varepsilon(\Delta\omega, 2\omega)$ [see (2)], which is, then, limited by g_{OB}. Further improvement can be obtained by decreasing g_m' effect together by decreasing Z_2. Note that cascoded MGTR (C-MGTR) is effective not only in reducing g_m'' by MGTR, but also in reducing g_m' effect and Z_2 by cascode configuration.

III. Fabrication Results

The 900 MHz C-MGTR RF amplifier whose schematic is shown in Fig. 1 is designed and fabricated using only CMOS in 0.35 μm SiGe BiCMOS process. The size of the MT is 360/0.35 μm and that of AT is 440/0.35 μm respectively. The MT is typically biased at gate drive ($V_{GT} = V_{gs} - V_{th}$, where $V_{th} = 0.66$ V) of 0.24 V and V_{GT} of AT is negative, i.e., AT is in subthreshold regime when there is no input signal.

Fig. 3 shows a microphotograph of the fabricated chip, whose size is 0.4×0.5 mm^2. Fig. 4 shows the measured IMD3 reduction versus V_{GT} of AT, while V_{GT} of MT is fixed at 0.24 V. Note that maximum IMD3 reduction as large as 20 dB is obtained.

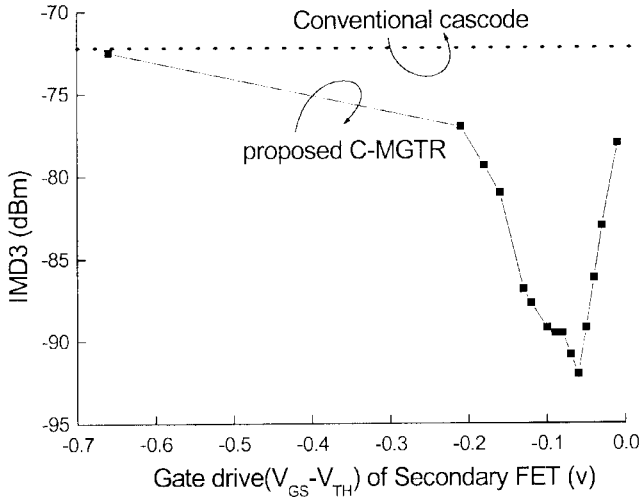

Fig. 4. IMD3 reduction versus ST gate drive bias.

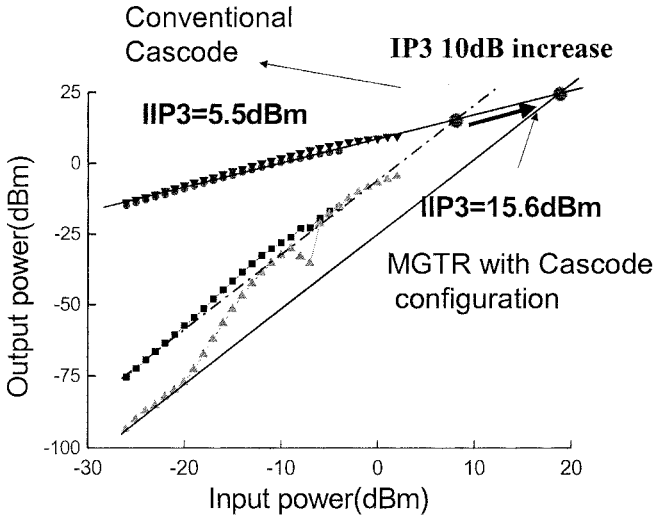

Fig. 5. IP3 comparison.

TABLE I
MEASURED PERFORMANCE COMPARISON

	Conventional cascode	MGTR with cascode
Gain	10 dB	10 dB
IIP3	5.5 dBm	15.6 dBm
Current	7.45 mA@Vdd=2.7 V	7.82 mA@Vdd= 2.7 V

Fig. 5 shows the measured IP3 at maximum IMD3 reduction. Note that IP3 improvement as large as 10 dB is obtained from proposed C-MGTR over 0.15 V range of V_{GT} which is wide enough to cover process variation.

The OIP3 of the proposed amplifier is 25.6 dBm at 7.8 mA current consumption. Measurement performance is summarized in Table I. Fig. 6 compares our noise figure versus normalized linearity performance results defined as

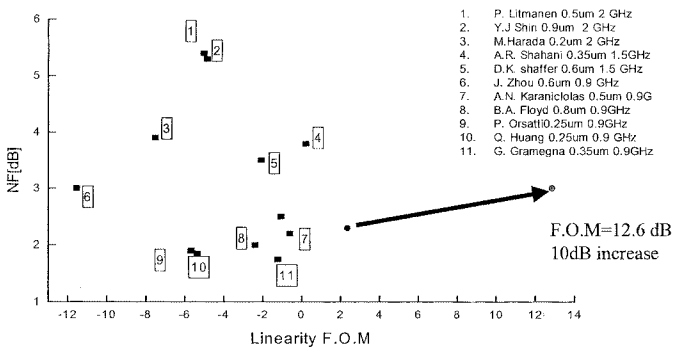

Fig. 6. Comparison of reported NF versus linearity figure of merit.

$10\log(OIP3\,(\mathrm{mW})/P_{dc}\,(\mathrm{mW}))$, F.O.M of linearity with those published in the literature. Although C-MGTR has slightly higher NF due to AT (note our NF is a simulated one), it improves normalized IIP3 by an order of magnitude of 10 dB.

Also this linearity F.O.M (12.6 dB) is higher than other transistor level linearization methods (10.3 dB in [6], 3.46 dB in ref. [7]). This is because those methods require additional power consuming circuits for linearization as explained in the introduction.

IV. CONCLUSION

A proposed C-MGTR CMOS RF amplifier is analyzed and measured. With MGTR, which linearize transconductance with canceling the negative peak value of g_m'' of the MT with the positive one in AT proper size and gate drive combined in parallel, g_m'' is effectively reduced, and further improvement is achieved in nonlinearity due to combination of g_m' and harmonic feedback by cascode configuration. The measurement result shows, compared with a conventional cascode amplifier, the proposed C-MGTR CMOS RF amplifier attains great linearity enhancement up to 10 dB at negligible extra power consumption.

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